

Interview Summary	Application No.	Applicant(s)	
	10/092,392	KATSAVOUNIDIS ET AL.	
	Examiner	Art Unit	
	Allen Wong	2621	

All participants (applicant, applicant's representative, PTO personnel):

- (1) Allen Wong. (3) Patent Agent David Wood.
 (2) Attorney David Klein. (4) _____.

Date of Interview: 02 May 2006.

Type: a) ☐ Telephonic b) ☐ Video Conference
 c) ☒ Personal [copy given to: 1) ☐ applicant 2) ☒ applicant's representative]

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☒ No.
 If Yes, brief description: _____.

Claim(s) discussed: 1, 11 and 22.

Identification of prior art discussed: Rhee (6,289,054), Glaise (6,097,725).

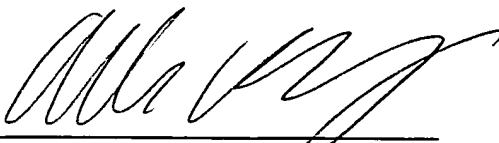
Agreement with respect to the claims f) ☐ was reached. g) ☒ was not reached. h) ☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Applicant's representatives discussed the differences of Rhee and Glaise verssus the present invention and also applicant's representatives discussed proposed amendments to claims that appear to overcome the prior art. But further search and consideration would be needed for the proposed amendments as attached.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.


 Examiner's signature, if required

AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in the Application.

Listing of Claims:

Claim 1 (Currently amended): A method of providing forward error correction (FEC) to a data frame, the method comprising the steps of:

packetizing the data frame into a plurality of frame packets, each frame packet having packet data defined by at least a first data portion and a second data portion;

selecting only said first data portions of packet data from each of the plurality of frame packets; ~~said selected portions being less than an entirety of a corresponding frame packet;~~ *for forward error correction exclusive of said second data portions*

simultaneously concatenating ~~only the~~ said selected first data portions of said packet data from ~~each of~~ the plurality of frame packets into a concatenated bit field;

generating a forward error correction code for the concatenated bit field of first data portions; ~~and~~

packetizing said forward error correction code to form a forward error correction code packet; and

*each of said transmitted
frame packets including said
first data portion &
said
second
portion*

transmitting ~~separately a packet containing the~~ said forward error correction
code and packet separately from the plurality of frame packets, ~~the packet~~
~~containing the~~ forward error correction code packet being identified with a user
data identifier code.

Claim 2 (Currently amended): The method as recited in claim 1, wherein the
transmission of the forward error correction code ~~in the separate~~ packet is MPEG-
4 compliant.

Claim 3 (Previously presented): The method as recited in claim 1, further
including the step of transmitting the plurality of frame packets temporally prior to
the separate forward error correction code packet transmitting step.

Claim 4 (Previously presented): The method as recited in claim 1, wherein the
forward error correction code generating step includes the step of generating the
forward error correction code as a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 5 (Previously presented): The method as recited in claim 1, wherein the
forward error correction code generating step includes the step of generating the
forward error correction code as a systematic code.

UNOFFICIAL - NOT FOR ENTRY

MR1035-1477

Amended Claims to Application SN 10/092,392

Claim 6 (Previously presented): The method as recited in claim 1, wherein the packetizing step includes the step of separating the packet data into at least portions respectively and separately containing motion vector data and Discrete Cosine Transform (DCT) data.

Claim 7 (Currently amended): The method as recited in claim 6, wherein the packet data selecting step includes the step of selecting as ~~the selected~~ first data portions of packet data only header data, the motion vector data and one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 8 (Currently amended): The method as recited in claim 1, wherein the packet data selecting step includes the step of selecting as ~~the selected~~ first data portions of packet data only packet data located between a resync field and a motion marker.

Claim 9 (Previously presented): The method as recited in claim 1, further comprising the steps of:

setting a flag indicating that a fixed Video Object Plane (VOP) increment is to set a fixed interval between each of the plurality of frame packets; and

assigning a fixed increment value to the fixed Video Object Plane increment.

Claim 10 (Currently amended): The method as recited in claim 1, further comprising the step of transmitting in the separate forward error correction code packet a value indicating a quantity of bits concatenated from ~~within at least a first packet of the plurality of frame packets for which the forward error correction~~ code is generated.

Claim 11 (Currently amended): An error correction generating circuit, comprising:

a processor coupled to a processor readable memory;

a first instruction sequence stored in the processor memory and operable to cause the processor to select ~~portions~~ only a first data portion of packet data from each of a plurality of frame packets of a corresponding packetized data frame, ~~each said selected portions being less than an entirety of a corresponding frame packet~~ having at least said first data portion and a second data portion;

a second instruction sequence stored in the processor readable memory and operable to cause the processor to ~~simultaneously~~ concatenate ~~only~~ the selected first data portions of packet data into a concatenated bit field;

UNOFFICIAL - NOT FOR ENTRY

MR1035-1477

Amended Claims to Application SN 10/092,392

a third instruction sequence stored in the processor readable memory and operable to cause the processor to generate forward error correction data for the concatenated bit field ^{said} of first data portions; *exclusion of said second data portions*

a fourth instruction sequence stored in the processor readable memory and operable to cause the processor to form a forward error correction packet and store the forward error correction data therein in a packet, said forward error correction packet being separate from the plurality of frame packets; and

a fifth instruction sequence stored in the processor readable memory and operable to cause the processor to identify the separate forward error correction packet with a data identifier code.

Claim 12 (Cancelled).

Claim 13 (Previously presented): The error correction generation circuit as recited in claim 11, further comprising a sixth instruction sequence stored in the processor readable memory and operable to cause the processor to set a flag indicating that a fixed Video Object Plane (VOP) increment is to set a fixed interval between each of the plurality of frame packets and to assign a fixed increment value thereto.

Claim 14 (Previously presented): The error correction generation circuit as recited in claim 11, further comprising a sixth instruction sequence stored in the processor

UNOFFICIAL - NOT FOR ENTRY

MR1035-1477

Amended Claims to Application SN 10/092,392

readable memory and operable to cause the processor to provide a Header

Extension Code (HEC) in every packet in a first sequence of packets.

Claim 15 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the error correction generation circuit is incorporated on an integrated circuit.

Claim 16 (Currently amended): The error correction generation circuit as recited in claim 11, wherein the ~~separate~~ forward error correction packet is MPEG-4 compliant.

Claim 17 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the forward error correction data is generated using a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 18 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the forward error correction data is generated using a systematic code.

Claim 19 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the packet data is separated into at least portions respectively

UNOFFICIAL - NOT FOR ENTRY

MR1035-1477

Amended Claims to Application SN 10/092,392

and separately containing motion vector data and Discrete Cosine Transform (DCT) data.

Claim 20 (Currently amended): The error correction generation circuit as recited in claim 19, wherein the selected first data portions of packet data includes only header data, the motion vector data and one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 21 (Currently amended): The error correction generation circuit as recited in claim 11, wherein the selected first data portions of packet data is only the packet data located between a resync field and a motion marker.

Claim 22 (Currently amended): An encoder circuit, comprising:

means for generating forward error correction data for a concatenated bit field formed ~~simultaneously~~ from only selected first data portions of packet data ^{exclusive of a second data portion} from each of a plurality of frame packets, where ~~the selected portions are less than an entirety of the corresponding each frame packet~~ has at least said first data portion and ^{said} a second data portion;

means for forming a forward error correction packet and storing the forward error correction data therein, said forward error correction a packet being separate from the plurality of frame packets; and

UNOFFICIAL - NOT FOR ENTRY

MR1035-1477

Amended Claims to Application SN 10/092,392

means for identifying the separate forward error correction packet with ~~an~~ a user data identifier code.

Claim 23 (Cancelled).

Claim 24 (Currently amended): The encoder as recited in claim 22, further comprising means for transmitting in the separate forward error correction packet at least a value indicating a quantity of bits concatenated from ~~within at least a first packet of~~ the plurality of frame packets for which forward error correction data was generated.